

Figure 1a

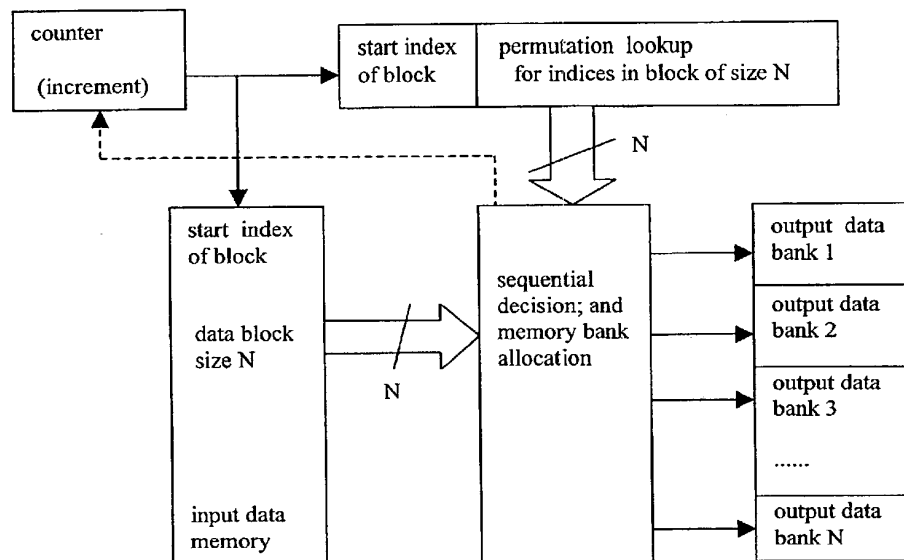


Figure 1b

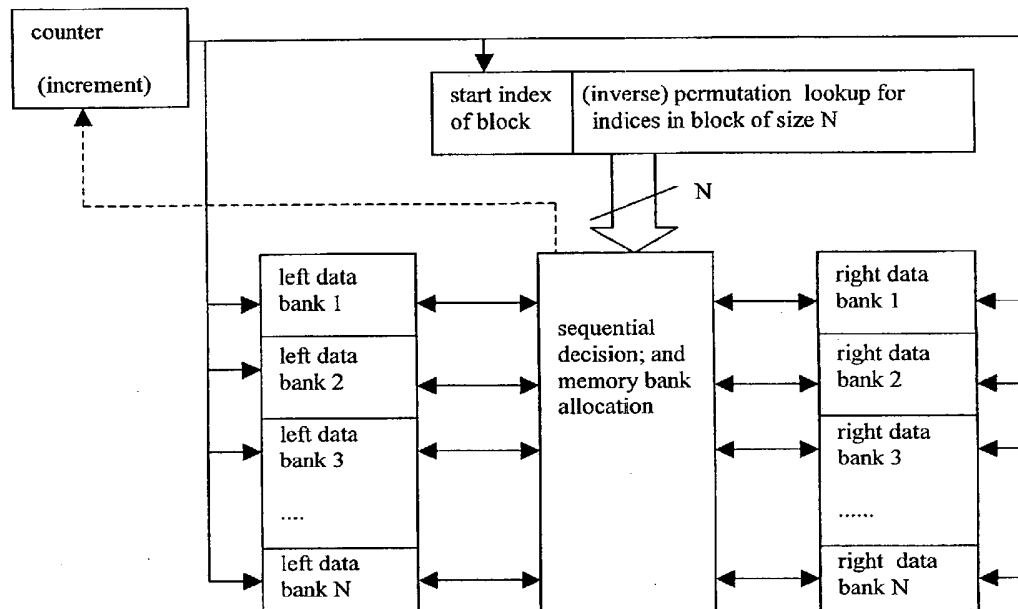


Figure 2a (prior art)

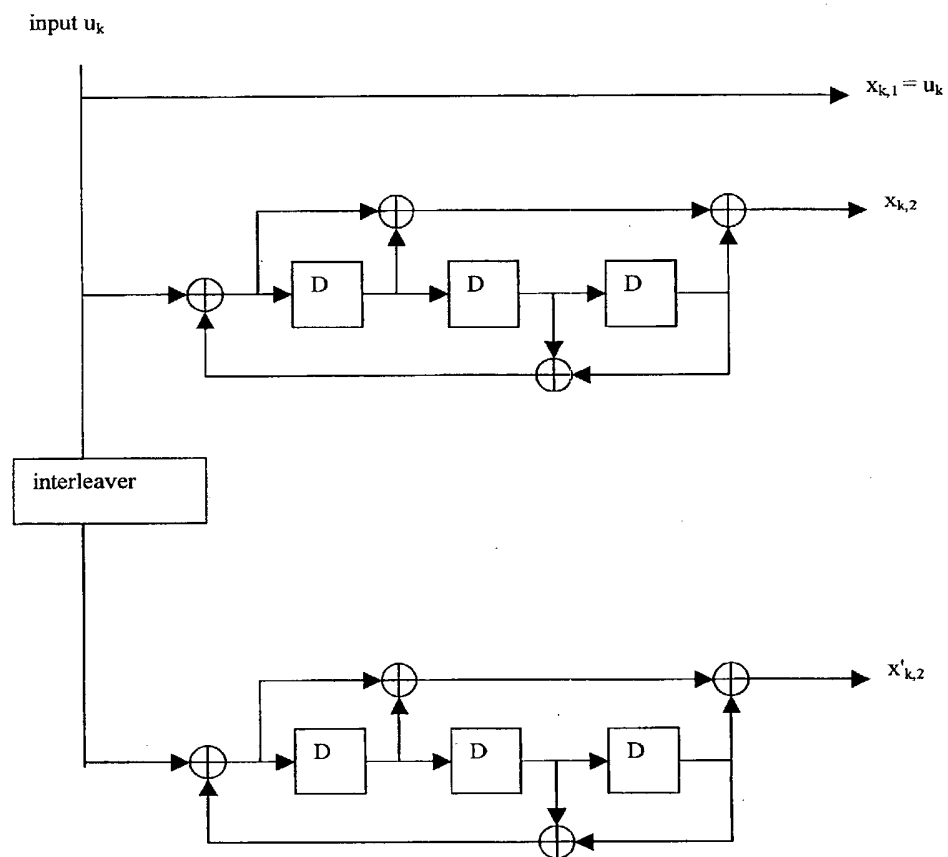


Figure 2b (prior art)

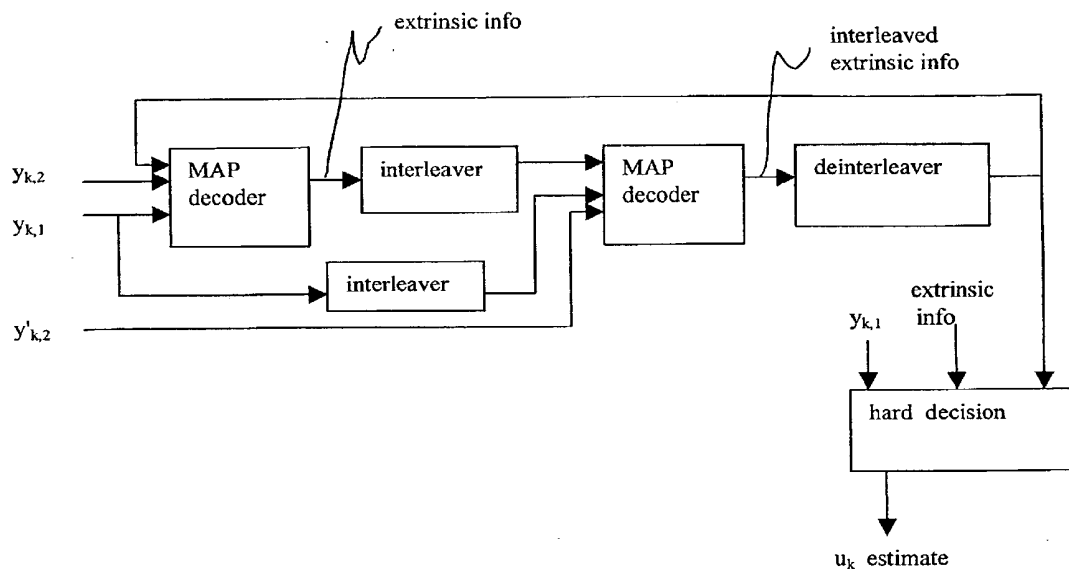


Figure 2c (prior art)

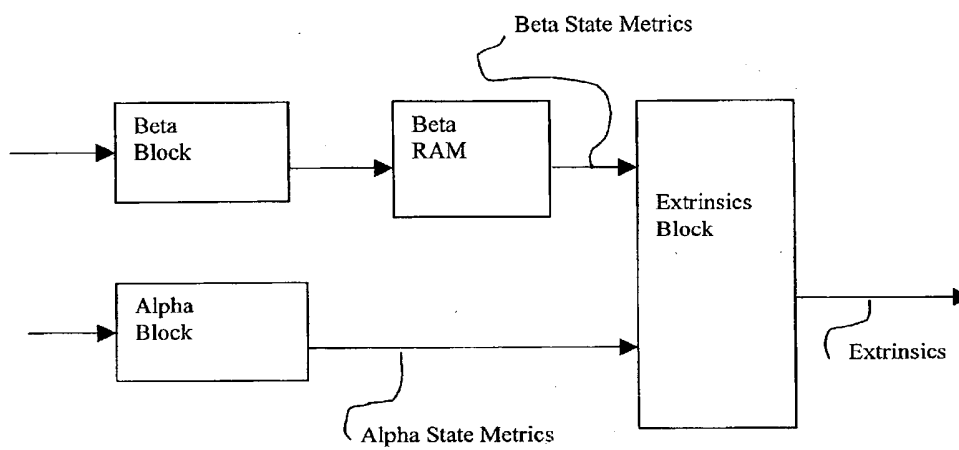


Figure 2d beta block (prior art)

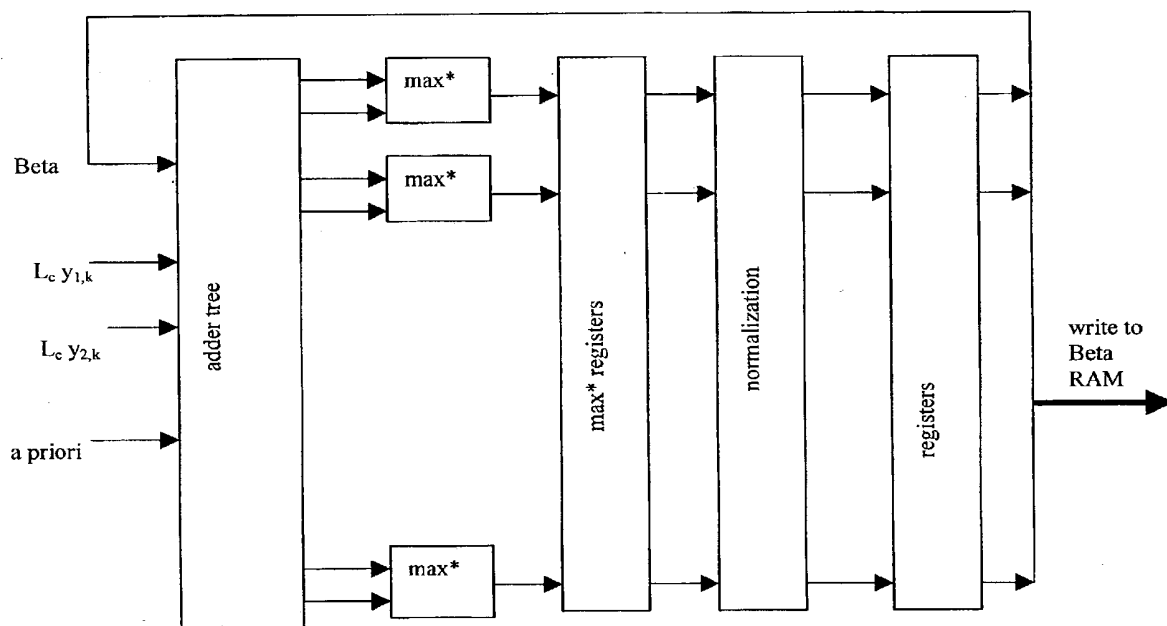


Figure 2e alpha block

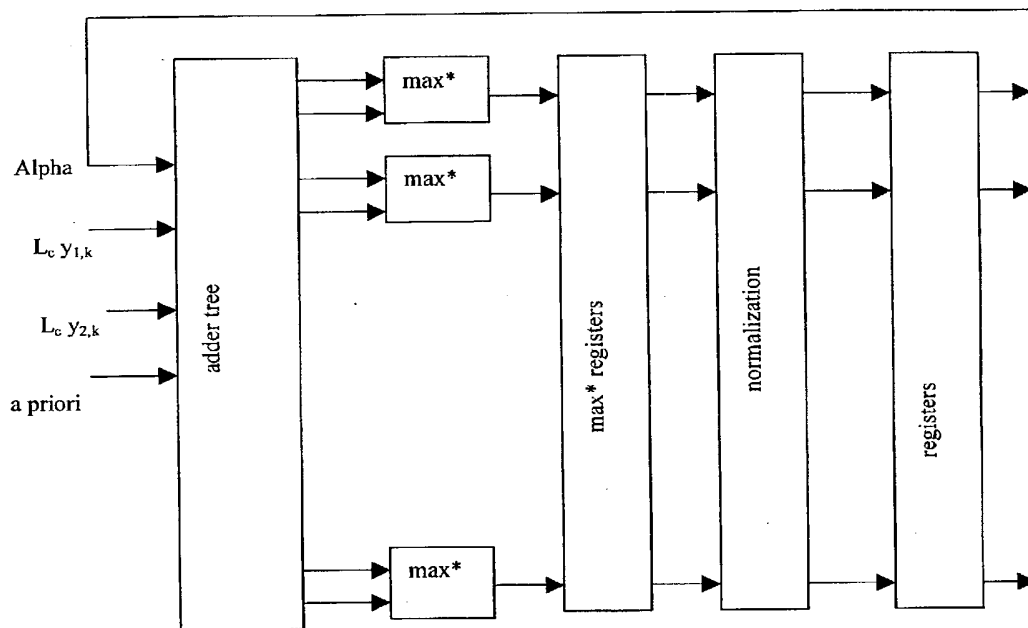


Figure 2f extrinsic block (prior art)

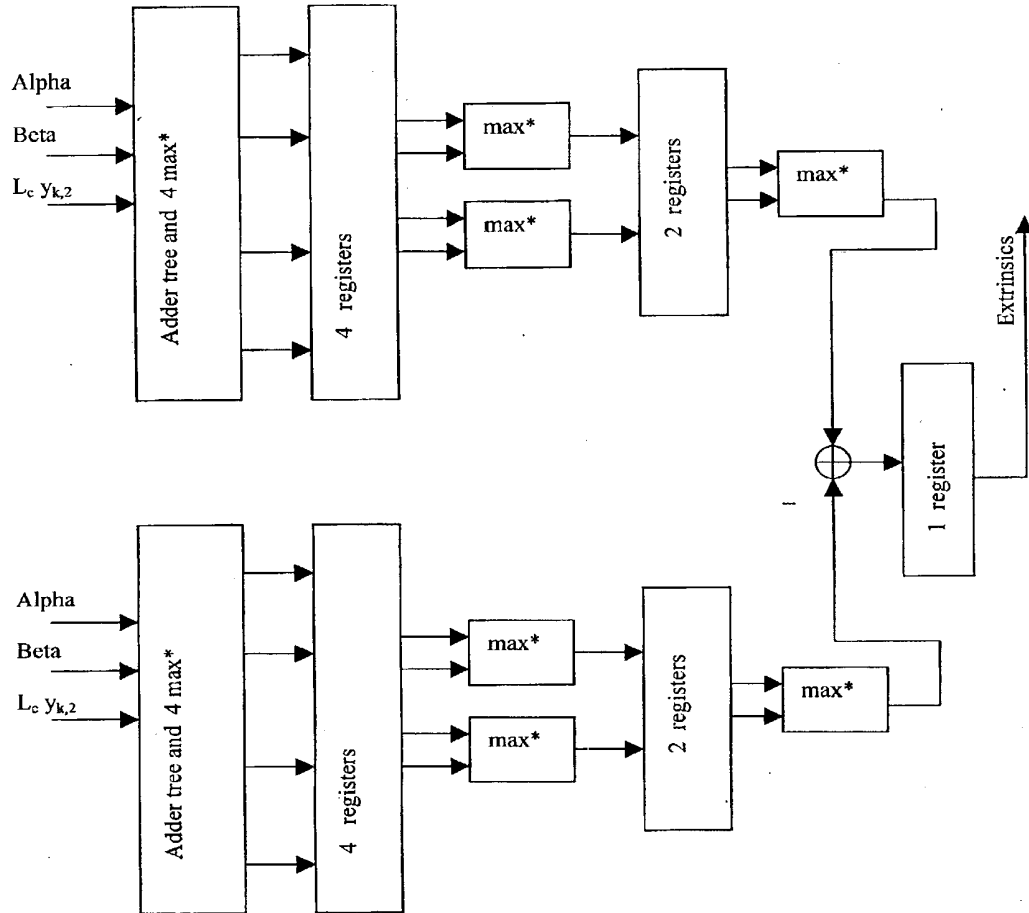
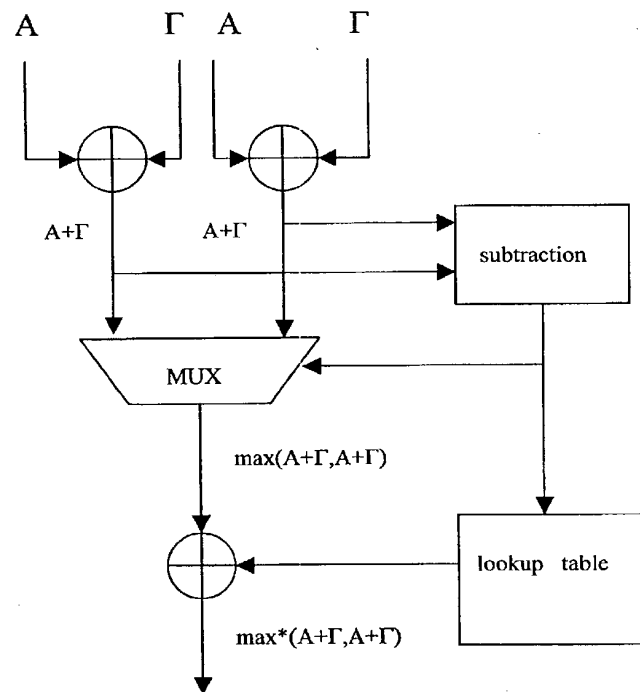


Figure 2g adder plus max* circuit (prior art)



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Figure 3a alpha block

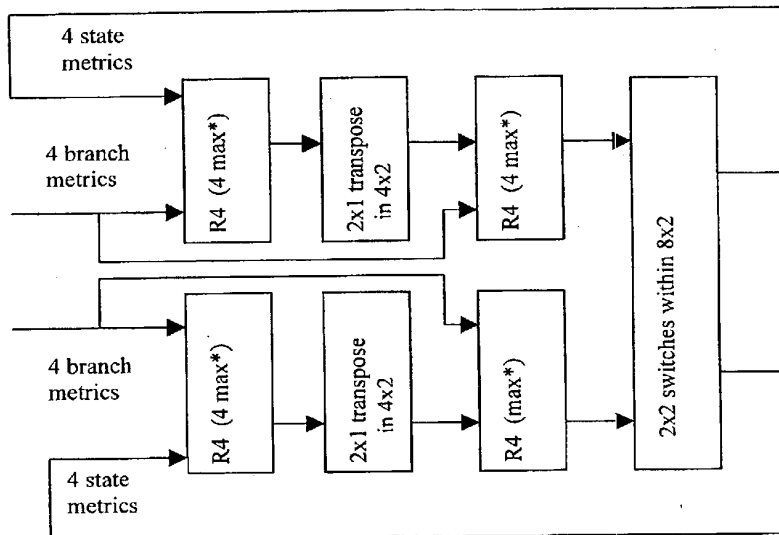


Figure 3b

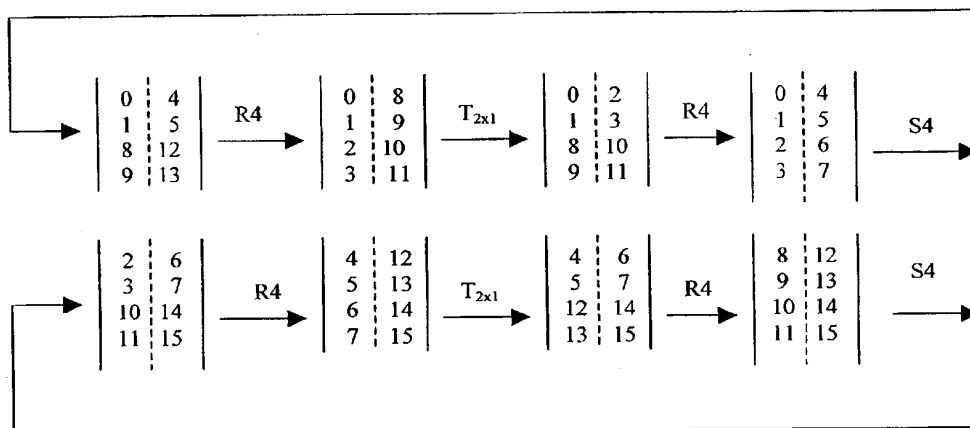


FIGURE 3c

Figure 3c first architecture beta block

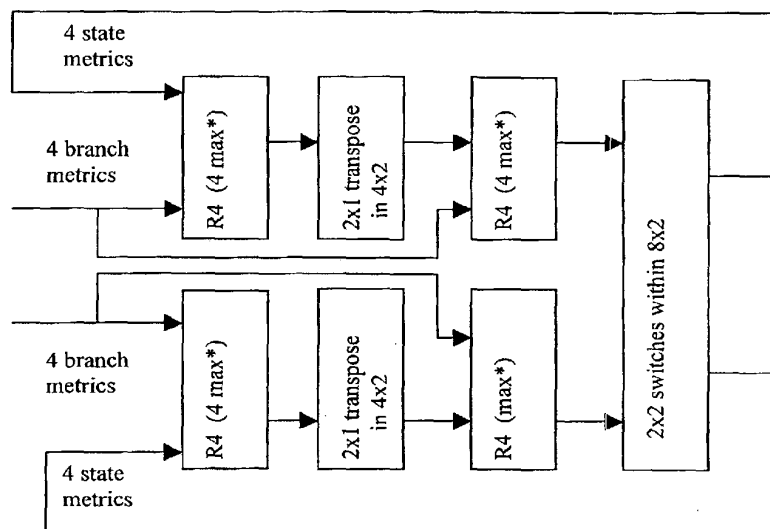


Figure 3d

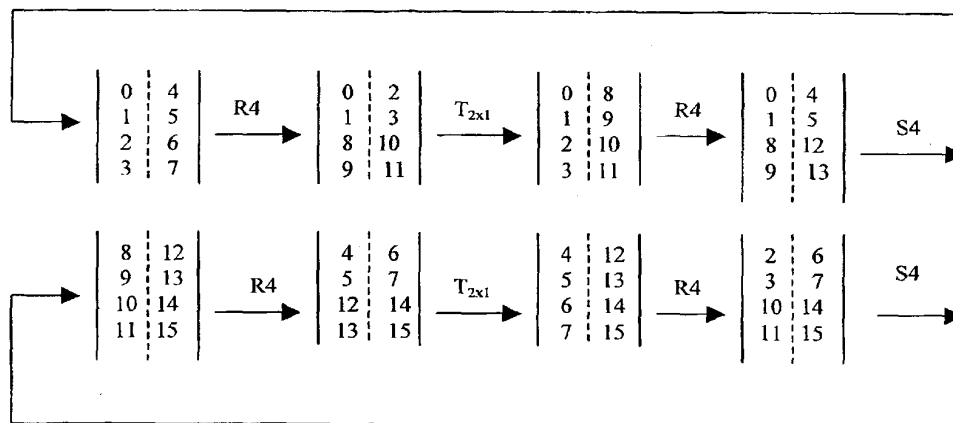


Figure 3e second architecture beta block

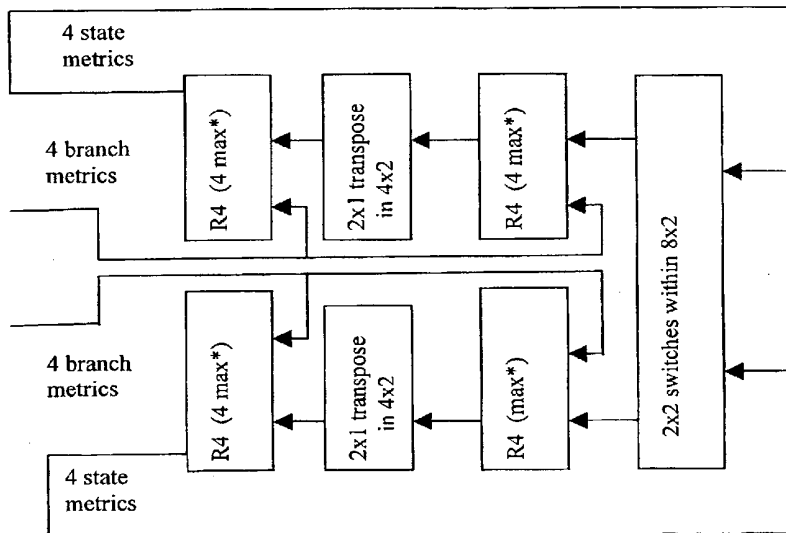


Figure 3f

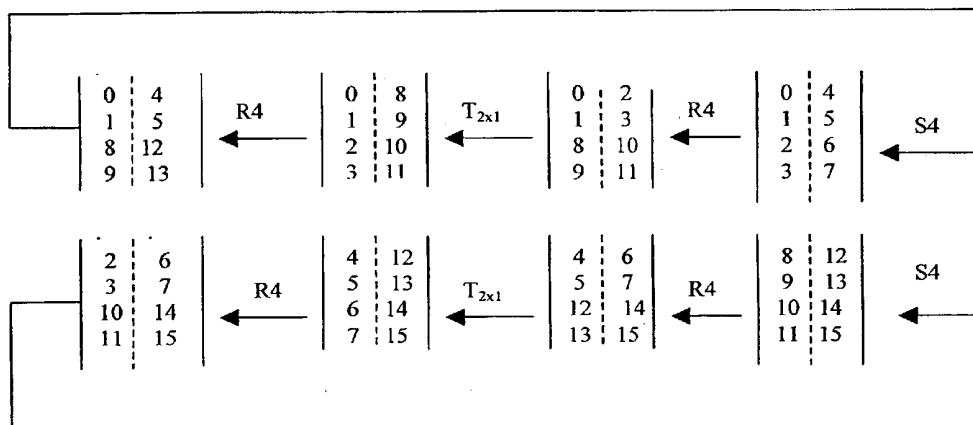


Figure 3g cascade extrinsic subblock

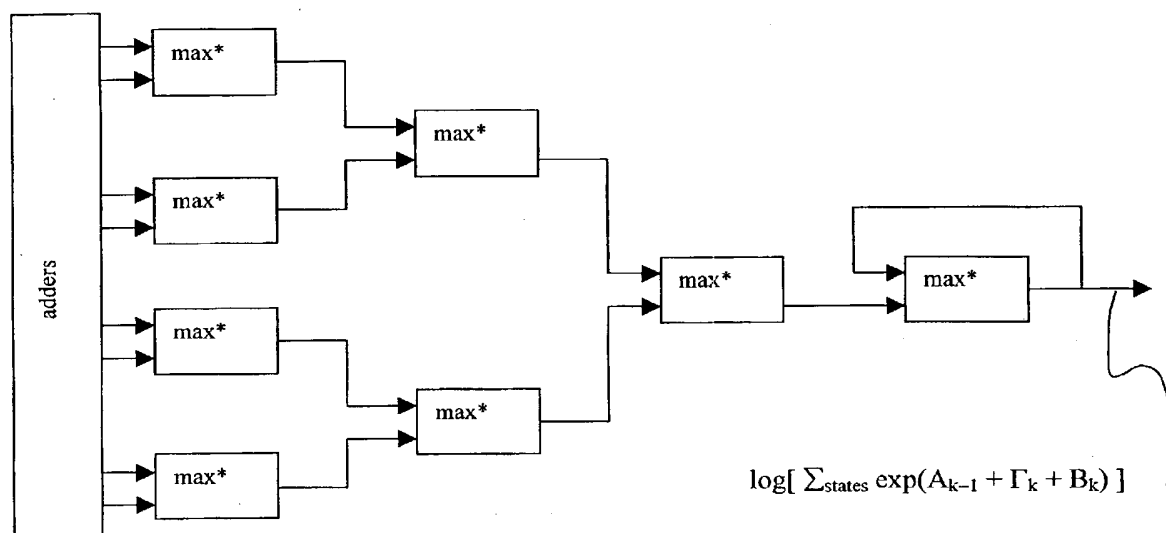


Figure 4 alpha block

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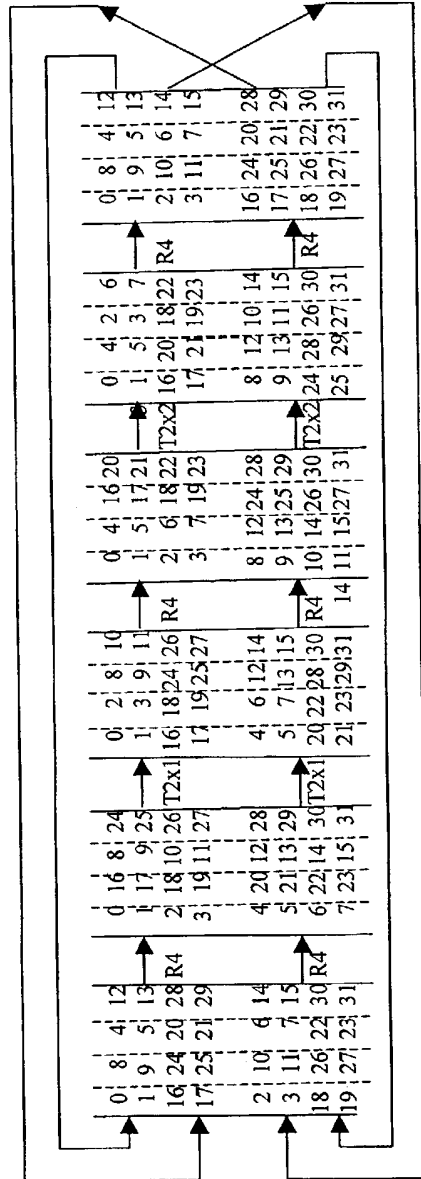


Figure 5a alpha block

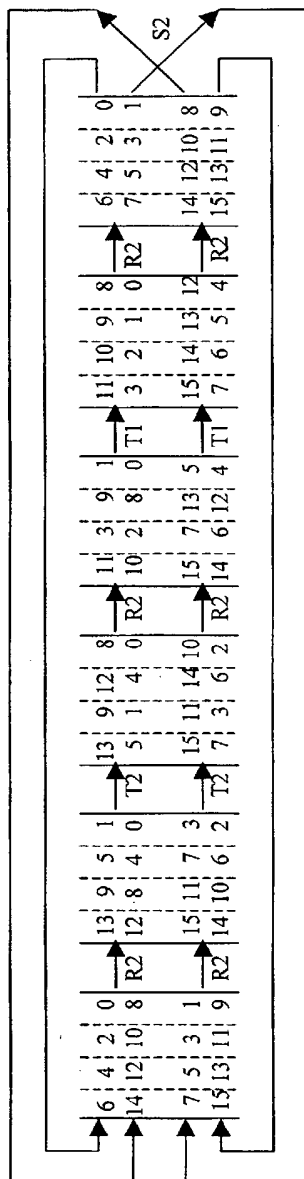


Figure 5b beta block

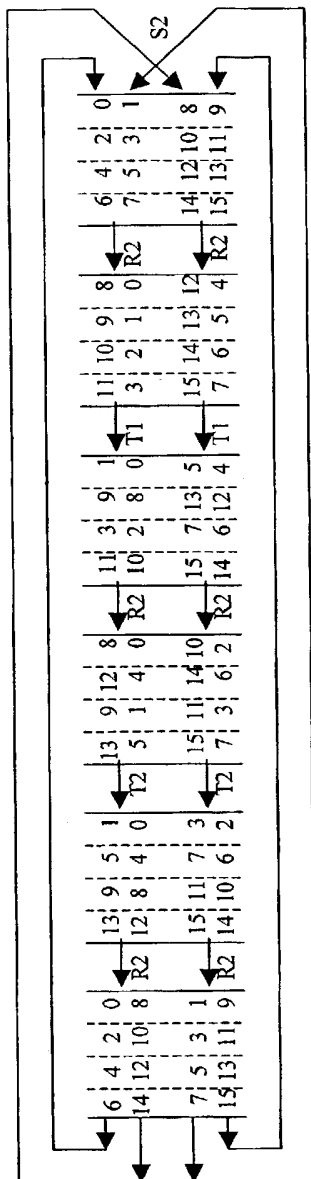


Figure 5c extrinsics block

